# Future Technology Challenges for Failure Analysis

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## Abstract

Failure analysis is a critical element in the integrated circuit manufacturing industry. This paper explores the challenges for IC failure analysis in the environment of present and future silicon IC technology trends, using the 1994 National Technology Roadmap for Semiconductors as a technology guide. Several advanced failure analysis techniques that meet the challenges imposed by the current state-of-the-art in integrated circuit technology are described and their applications are discussed. New paradigms will be required for failure analysis to keep pace with the future advancements in integrated circuit technology.

FAILURE ANALYSIS IS A CRITICAL ELEMENT during all phases of the integrated circuit (IC) product cycle. The goal of failure analysis (FA) is to determine the root cause of a failure or parameter excursion so that corrective action can be taken. In the broadest sense, FA includes support of fabrication tool development, processing development, technology development, manufacturing, testing, and field return analysis of ICs. A broad definition of FA includes physical materials analysis as well as electrically oriented defect localization. FA is performed on unpatterned test wafers, short loop monitor wafers, test circuits on completely processed wafers, IC die, and packaged ICs. Because of the level of complexity of current IC technologies, test structures are often substituted for ICs during development to facilitate yield analysis. In this case, the surrogate test structures must dependably predict effects that will be manifested in the IC.

As IC technology advances, FA technology must keep pace if it is to provide the needed level of support. A clear roadmap of where IC technology is headed is a prerequisite for guiding the research and development activities needed to provide the matching advancements in FA technology. The 1994 National Technology Roadmap for Semiconductors (NTRS) (1), published by the Semiconductor Industry Association, provides a 15 year projection of technology trends for leading edge ICs. Table 1 shows selected technology characteristics from the 1994 NTRS for the years 1995 and 2001. A six year projection is a reasonable point of comparison and provides an appropriately advanced technology target as a driving force for the development of advanced FA techniques. Other relevant technology characteristics are the increasing use of completely planarized surfaces and upper wiring levels as power distribution planes. The NTRS also addresses trends toward higher density packaging technologies including smaller package profiles and MCMs (multichip modules). MCM technology introduces a host of challenges for FA, but we will address only flip chip technology in this paper.

| **Characteristic** | **1995** | **2001** |
|---|---|---|
| wafer size | 200mm | 300mm |
| die size (DRAM) | 250mm$^2$ | 360mm$^2$ |
| feature size | 0.35mm | 0.18mm |
| wiring levels | 4 - 5 | 5 - 6 |
| bits/chip (DRAM) | 64M | 1G |
| clock frequency | 150mhz | 300MHz |
| operating voltage | 3.3V | 1.8V |
| chip I/Os | 900 | 2000 |

Table 1. Selected technology characteristics from the NTRS (1).

In this paper we review developments in failure analysis tools and techniques that help meet the challenges presented by state-of-the-art IC and packaging technologies. Examples include advanced scanning electron beam, scanning photon beam, scanning probe, light emission, and thermal imaging techniques. Such techniques may enable analysis of circuits where, for example, additional interconnection levels, power distribution planes, or flip chip packaging completely eliminate the possibility of employing standard optical or voltage contrast failure analysis techniques without destructive deprocessing.

New paradigms for failure analysis will be needed to meet the challenges posed by the billion transistor ICs that are anticipated by the NTRS. These new paradigms include the networking of FA apparatus, the incorporation of design for FA, the development of software techniques for defect localization and root cause analysis using only electrical test data, and the employment of knowledge-based systems.

The focus of this paper is primarily on defect localization using techniques based on advanced imaging and on the interaction of various probes with the electrical behavior of devices and defects. The challenges that technology advancement poses for detailed materials characterization using physical, chemical, and optical techniques are not discussed here since they have been reviewed thoroughly elsewhere (2, Diebold 1994).

## Imaging Techniques

**Optical Microscopy.** Optical microscopy techniques are able to locate many physical defects and have been a mainstay in FA for years. However, smaller feature sizes are pushing optical microscopy towards its resolution limit, around 0.2 - 0.3 mm using visible light. Other technology trends that have a large impact on optical microscopy include additional interconnection levels, power distribution planes, and flip chip packaging. Obviously, an optical image from the top of an IC reveals few features deep in the structure if there are many interconnection levels and power distribution planes which obscure a large percentage of the IC surface. Scanning optical microscopy (SOM) provides improved image resolution and contrast compared to conventional optical microscopy. The use of IR lasers extends the usefulness of the SOM by permitting observation through the wafer. Images of the active regions of an IC can be obtained using reflected IR microscopy from the back of the die with a resolution of resolution about 0.6 mm. This circumvents problems caused by additional interconnection levels, power distribution planes, and flip chip packaging.

**Scanning Electron Microscopy.** As IC feature sizes decrease and defects of smaller size become more important, imaging techniques with higher resolution than optical microscopy are required. For the 0.18 mm feature technology in year 2001, the maximum allowable particle defect size is 60nm. SE Secondary electron (SE) imaging in a field emission scanning electron microscope (FESEM) generates a high resolution (2-5 nm depending on beam energy), large depth of field image that depicts the surface topography of an IC. FESEMs have excellent spatial resolution at low beam energies, allowing nondestructive imaging of in-process wafers and high resolution imaging of insulating layers without charging problems. The change in secondary electron emission with material is also pronounced at low beam energies, so different layers in a cross-section can be identified in a FESEM without using special wet or dry etches to produce topology differences.

Although SE imaging in the FESEM will not have difficulty resolving features the size of future lateral IC dimensions, the increasing use of planarization techniques negates the effectiveness of SEM imaging. Unless deprocessing approaches are employed, SEM images of planarized surfaces will provide little information. The vertical dimensions which must be imaged in cross-sections have already decreased to near the FESEM resolution limits, and defects that can cause failure in these films may be smaller yet. Detailed root cause analysis may require the use of a transmission electron microscope (TEM), which provides resolution down to the atomic scale..

**Scanning Probe Microscopy.** Scanning probe microscopy (SPM) is a rapidly growing field that is just beginning to have an impact in the FA of ICs. Samples are imaged in an SPM by scanning a sharp probe tip in close proximity to the sample surface and detecting the interactions between the tip and the sample. Scanning probe instruments provide an entirely new capability for topographical imaging of submicron structures, extending spatial resolution well beyond the limits of optical tools. Scanning tunneling microscopy (STM) provides topographic imaging of conductive surfaces with resolution to the atomic level. Atomic force microscopy (AFM) provides a topographical map of conducting or insulating surfaces with resolution also to the atomic level (20). AFM has recently been used to image IC cross-sections with nanometer resolution, better than that obtainable with optical microscopy or SEM (21). Scanning near-field optical microscopy (SNOM) combines optical and scanning probe technologies and can image surfaces on a scale well beyond the classical diffraction limit (Betzig & Trautman).

**Focused Ion Beam.** The capabilities of focused ion beam (FIB) systems are rapidly becoming critical for FA of submicron technology ICs. FIB systems use a focused beam of $Ga^+$ ions for imaging, milling, etching, and deposition of metals and dielectrics (27,28). No other tools provide these capabilities with sufficient spatial control to effectively support technologies with 0.18mm feature sizes.

FIB system ion milling and imaging enables in-situ cross sections, an effective approach for analyzing the root cause of a failure. Sequential cross sections can be made through a feature of interest. Upper layers of an IC may be milled away to expose underlying layers for mechanical or electrical analysis, and conductors may be cut to isolate interconnections and devices.

FIB systems also can be used to precisely deposit conductors and dielectrics, enabling local modifications in the electrical interconnections of the IC and the deposition of additional contact areas that can be used to probe circuit functions and measure voltages on functioning ICs (30).

## Techniques Based on Electrical Stimulation

Larger IC die sizes and higher integration levels have made FA impossible using purely physical techniques. There is simply too much silicon circuitry to analyze. Even for test circuits and short loop monitors, it is not cost effective to apply only physical analysis techniques. Powerful FA techniques based on the application of internal IC probing using electron beam, optical beam, and scanning probe techniques combined with electrical stimulation at the IC pins have enabled dramatic improvements in rapid defect localization. In many cases the level of integration of the IC is not an important factor in quickly isolating the defect.

Technology trends that have a significant impact on FA techniques using electrical stimulation are higher clock frequencies, lower operating voltages, and increased I/O pin counts. These trends dictate the use of higher performance test equipment and enhancement of the electrical interconnection between the tester and the FA apparatus.

**Light Emission.** Light emission (LE) analysis is often the primary tool for localizing many types of common IC defects on large die with small feature sizes and high integration levels. LE is effective in identifying gate oxide shorts, degraded pn junctions, and MOS transistors in saturation due to interconnection shorts and open circuit defects (12). LE performed using extensive test vector sets enables rapid localization of all light emitting defects on an IC at low magnification, independent of feature size, and subsequent high magnification examination links the emission sites to circuit features. Because the emitted photons have energies in both the visible and near IR wavelengths, the light emission can be observed from the backside of the die, circumventing optical obscuration caused by additional interconnection levels, power distribution planes, and flip chip packaging. Figure 1 shows *a low magnification light emission image of a 1.25 mm feature size, two level metal, 32-bit microprocessor with four gate oxide shorts (highlighted by the four white boxes).* (***Get a better example with smaller feature size-Intel FA work)***

**FIGURE 1.** Low magnification light emission microscopy image showing four gate oxide shorts (bright areas in the four boxes) in a 32-bit microprocessor.

**Voltage Contrast.** Electron beam voltage contrast (VC) techniques, also known as electron beam testing, have an important role in FA since they provide nondestructive methods for observing internal IC operation and the electrical effects of defects. Advanced electron beam test systems provide integration of CAD databases and permit comparison of control and failing devices through image processing. Software tools are available that reduce the time to locate and analyze logical faults through an automated backtracing approach (16). Evolutionary improvements in electron beam test equipment will continue, providing better voltage, timing, and spatial resolution as well as more powerful software control. However, there are fundamental limitations imposed by advances in IC technology that must be addressed in order for VC to remain useful.

The most obvious challenge is simply dealing with the complexities introduced by larger die sizes, smaller feature sizes, and higher integration levels. Advances in software for navigation, test point selection, and data analysis will be needed. The decreasing feature sizes also result in more interference from adjacent conductors in the VC measurements. Higher clock frequencies and lower operating voltages will necessitate development of faster electron beam gating and more sensitive SE energy spectrometers. Perhaps the most difficult challenge is posed by the increasing number of interconnection levels and the use of the upper metallization level or levels as power planes. The shielding effect of these wiring levels will render VC analysis ineffective on fully processed ICs without deprocessing. Solutions to this problem include designed-in internal test points on the topmost metallization layer and the use of a FIB system to open vias to lower levels or create probe pads at the point of interest. It appears that a design for FA philosophy will be necessary in order to maintain the utility of VC for analyzing the circuits of the future.

**Charge-Induced Voltage Alteration and Light-Induced Voltage Alteration.** Charge-Induced Voltage Alteration (CIVA) (17) and Light-Induced Voltage Alteration (LIVA) (18) are techniques which provide a fast, simple method for locating open conductor, contact, via, and junction defects. Open circuit failures traditionally have been very difficult to localize in complex ICs since the failure signature is not obvious. CIVA and LIVA simplify localization of these defects on an entire IC in a single, low magnification image, independent of feature size, with the ability to zoom in an correlate the defect site to circuit features. Both techniques employ the same electrical approach but use different probes: CIVA employs an electron beam while LIVA uses a photon beam.

CIVA analysis circumvents many of the challenges of IC technology advancement. CIVA may be performed through multiple layers of dielectrics and metals by increasing the electron energy, but care must be exercised to avoid irradiation damage to the IC. Figure 2 shows an example of low magnification CIVA imaging of a 1 mm feature size, passivated, two-level metal gate array with an open metal conductor. The CIVA image (bright white lines) of the conductor network that is open circuited is superimposed on a secondary electron image.

**FIGURE 2.** Low magnification CIVA image of an open conductor network (bright white) superimposed on a SEM image of a gate array IC.

CIVA may be performed nondestructively on fully processed ICs using low electron beam energies. This technique is called low energy CIVA (LECIVA) (19). Figure 3 shows a low magnification LECIVA image of the conductor network connected to an open level two to level three via on a 0.8 mm feature size, three-level-metal Intel 486 microprocessor. Application of LECIVA is subject to the same limitations that apply in VC, since lower conductor levels may be analyzed only if they are not covered by other metal layers.

**FIGURE 3.** Low magnification LECIVA image of conductors connected to an open via (bright area in box) superimposed on a SEM image of an Intel 486 microprocessor.

LIVA uses a SOM to quickly localize either defective *pn* junctions or biased junctions that are electrically connected to defects such as open circuits (18). LIVA can also identify the logic states of transistors with much greater sensitivity than other optical techniques. LIVA analysis is performed from the front of an IC die using a visible laser or from the back of the die using an infrared laser. Figure 4(a) shows a backside IR SOM image of an I/O port region of a 1.25 mm feature size, two level metal microcontroller, and Figure 4(b) shows the backside LIVA logic state image when the port is in the "1" state. The dark contrast areas indicate p-channel transistors that are "off". The “fuzzyness” of the image results from the diffusion length of the optically generated electrons and holes. Note that the transistors in the image are completely covered by level two metal, so no front side imaging or logic state analysis is possible.

**FIGURE 4(a).** Backside IR SOM image of an I/O port on a microcontroller.

**FIGURE 4(b).** Backside LIVA logic state image of the I/O port shown in Figure 4(a).

**Scanning Probe Techniques.** In addition to imaging, SPM techniques have been used to measure internal voltages and currents on ICs. Charge force microscopy (CFM) can perform potentiometry within ICs with sub-millivolt sensitivity, and has also been applied to develop an AFM-based voltage contrast technique for measuring voltage waveforms up to 20 GHz (22). Magnetic force microscopy (MFM) uses a magnetized tip to detect magnetic field gradients. MFM current contrast imaging can analyze internal IC currents with a sensitivity of ~ 1 mA dc and ~1 mA ac (23). The combination of CFM and MFM in a single instrument may enable simultaneous measurement of internal IC voltages and currents. CFM will experience technological limitations similar to those discussed for VC analysis, while MFM will suffer lower spatial resolution due to the long range of magnetic forces. However, MFM should be capable of detecting currents on conductors located beneath other conductors for the same reason. *Figure 5(a) shows an optical micrograph of two metal interconnections on a test structure; the white box indicates the area scanned for the MFM/CCI image shown*

*in Figure 5(b).* A 10 mA ac square wave is applied to the right interconnection and its phase is shifted halfway through the top-to-bottom scan. The contrast in Figure 5(b), which indicates the magnetic force applied to the MFM tip, reverses when the phase shift occurs. The left interconnection is not electrically driven and its topography is imaged due to Van der Waals forces.

*eliminate??*

**FIGURE 5(a).** Optical micrograph of two interconnections on a test structure; the white box is the area scanned for MFM/CCI.

**FIGURE 5(b).** MFM/CCI image of the two conductors in Figure 5(a) showing contrast from a 10 mA square wave current in the right conductor.

**Focused Ion Beam Techniques.** If electrical feedthroughs are provided in the FIB chamber, electrical measurements may be used for in-situ monitoring of IC modification and voltage contrast imaging may be employed for FA (Campbell and Soden).

**Thermal Imaging.** Thermal imaging techniques are helpful in defect localization when there are no obvious detectable symptoms such as light emission or CIVA/LIVA signals. Thermal imaging techniques rely on detecting a defect on an operating IC through a local temperature increase caused by increased power dissipation. These techniques are generally unaffected by feature size, integration level, number of interconnection levels, and planarization. However, thermal conductivity may cause a somewhat diffuse "hot spot" and the spatial resolution of the imaging system may not be the limiting factor in defect localization.

Liquid crystal techniques are commonly used for "hot spot" detection. The spatial resolution and temperature resolution of this technique are relatively poor, and there is no temperature mapping capability. Infrared thermography provides a temperature map of the IC surface with good temperature resolution. However, the spatial resolution is relatively poor. Fluorescent microthermographic imaging (FMI) uses the temperature dependent fluorescence quantum yield of a rare earth chelate to provide a direct, quantitative measurement of surface temperature (26). This technique has excellent spatial and temperature resolution, and research to improve the technique is ongoing (Tangyunyong and Barton).

## New Paradigms in Failure Analysis

**Failure Analysis Using Only Electrical Test Data.** Leaving the traditional approach of performing FA behind and embracing the concept of performing automatic analysis of defects using only the electrical test data available at the I/Os of the IC is indeed a paradigm shift. The NTRS identifies the need for improvements in defect modeling, automatic test vector generation, utilization of $I_{DDQ}$, boundary scan and full scan techniques, and incorporation of built-in-self-test in order to achieve it.

Recently, a new defect class model has been developed that inherently links to the circuit architecture and moves away from the classic stuck-at fault model that postulates abstract representations of defects (ITC94). This model also provides guidance for maximum defect coverage with a minimum of test vectors. Parametric testing techniques for CMOS IC diagnosis are becoming more ubiquitous. In addition to increased defect and fault coverage, $I_{DDQ}$ testing enables rapid identification and physical localization of many design, layout, and fabrication problems (4). Software tools have been written that relate $I_{DDQ}$ test vectors to logic fault and physical defect localization (5,6).

**Design for FA and Defect Diagnosis.** As IC complexity evolved, it reached the point where it became imperative for circuit designers to consider testability early in the product concept stages. This occurred because of the high cost of inadequately testing the IC, including the risk of missing critical time to market deadlines and ultimately failure to manufacture the product. It was found that the test cost could be reduced only by bringing together the design and test activities. Design for testability is now an established practice, a successful example of concurrent engineering. Continued advances in complexity and reduction in the IC manufacturing cycle time now make design for FA an equally critical process. Work teams that include design, test, and FA personnel must be formed early to assure that IC defects can be successfully diagnosed quickly and efficiently. Approaches to designing for FA Test pattern generation or selection approaches based on more realistic models provide the capability to map from failing test vectors to physical structures based on netlist and layout information.

Benefits from incorporating design for FA occur immediately, resulting in the ability to detect design problems during simulation and test pattern generation, analysis of first production wafer lots, as well as throughout the product life cycle. Designing for FA adds value to the manufacturing process in a variety of ways. A fundamental purpose is to enable real time diagnosis during production testing of wafers. The ability to rank order the occurrence of "killer" defects, by type and location, with minimal or no impact on production throughput is a vital outcome. This provides the information needed to immediately evaluate and implement corrective action in IC fabrication. Closing the loop with this critical information is the best approach for product yield enhancement that cannot be achieved with in-line test structures and monitors.

Approaches to designing for FA involve diagnostic software and IC design concepts. Software issues include moving away from models, such as the stuck-at fault, that are abstract representations with no relationship to the physical layout to defect models or classes that inherently link to the circuit architecture (8). Test pattern generation or selection approaches based on more realistic models provide the capability to map from failing test vectors to physical structures, based on netlist and layout information. Merging defect classes with improved algorithms for fault dictionaries created during simulation is necessary for diagnosis (9). IC design for FA concepts include extension of techniques that improve controllability and observability, such as partitioning and on-chip self test circuitry.

**Networking of Failure Analysis Equipment.** Larger die, higher integration levels, completely planarized surfaces, additional interconnection levels, and power distribution planes all create navigation difficulties while performing FA. CAD navigation software is typically provided on electron beam probe systems and can be installed on focused ion beam systems and other FA equipment. This software links layout and schematic information from the CAD database with images and internal probe data from the FA tools. Linkage assists in positioning probes at the point of interest and correlating the defect site to its physical and electrical location. However, full integration throughout the FA laboratory is

uncommon. Further utilization of the CAD database, such as providing cross-sectional diagrams of any point on the IC, will greatly assist the failure analyst. Ultimately, networking of all the FA tools in the laboratory and linking with the design and test databases will be required for effective FA.

**Failure Analysis Information Systems.** FA is a multidisciplinary activity. The effective failure analyst must understand circuit design, IC architecture, semiconductor device physics, IC processing, and IC testing. This broad set of skills takes years to acquire, perhaps through rotational assignments in different departments of a company, while constant advances in technology further complicate the process. Analyst training is usually accomplished on the job and through conference attendance, since few universities provide applicable laboratory experience. There are several short courses and seminars that provide useful general information, but the depth of coverage may be insufficient to provide immediate help back at the workplace. FA books also have broad applicability, but rapidly become dated as technology advances.

A new paradigm for training failure analysts is the use of failure analysis databases, hypertext help systems, and expert systems. These software products also add value by preserving the knowledge of experienced failure analysts, which is usually lost through retirement or job change. A large “smart database” has been described that uses all of a company’s FA records to provide a prediction of the failure mechanism and a proposed FA course of action (31). Interactive FA expert systems have been implemented to help train inexperienced analysts as well as guide and assist experienced analysts while performing analyses (32,33). One limitation is the time and effort necessary to test and debug these systems. Because of this limitation researchers have begun to look at other ways to deliver FA information. The World Wide Web (a graphical, hypertext view of the Internet) is one option under development that will provide up-to-date, comprehensive multi-media information and training to analysts at their work locations.

As computer technology continues to evolve and network bandwidth increases, multimedia training will become more prevalent. Failure analysts will be able to receive audio instructions for FA procedures. For example, the analyst can have the computer audibly dictate instructions on how to perform a wet chemical etch. The analyst will not have to type on a keyboard or read a computer screen while the etch is being performed. Failure analysts will also watch conputerized video clips that describe such procedures as how to delid an integrated circuit, or how to bring up the electron beam on a new scanning electron microscope.

## Conclusions

FA in today's IC industry is squeezed between the need for very rapid analysis to support manufacturing and the exploding complexity of IC technology. A number of advanced techniques and tools have been developed which have enabled FA to keep pace with technology. However, the technology roadmap for the future poses such large challenges that new paradigms for FA must be realized Continued support for research on new FA technologies and for innovative new approaches to FA is a critical requirement for the future.

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